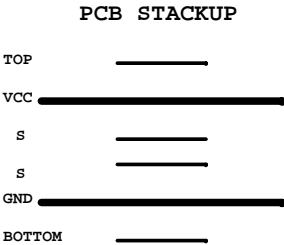
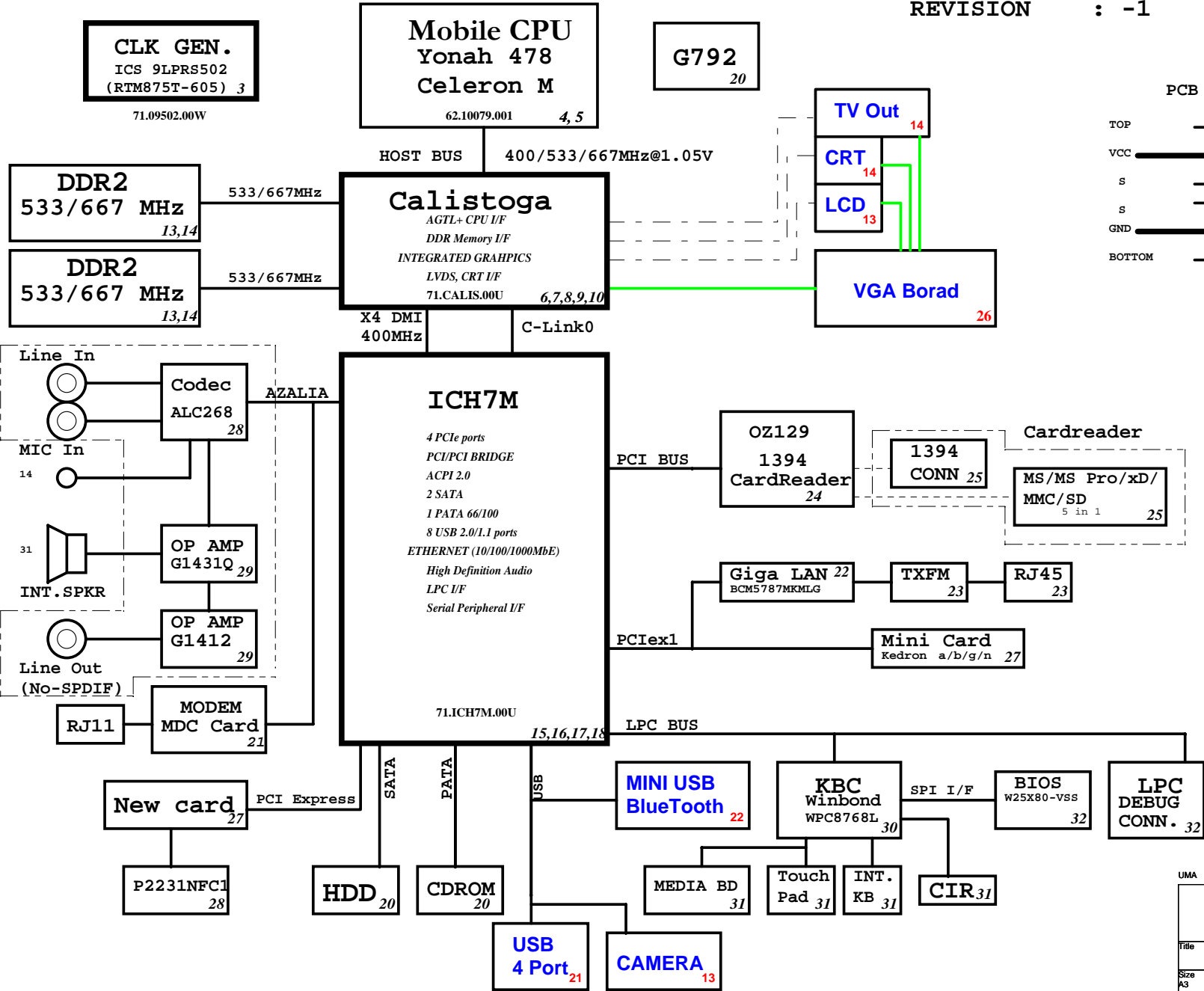


Volvi Block Diagram

Project code: 91.4U701.001
PCB P/N : 07200
REVISION : -1



SYSTEM DC/DC MAX8744 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5
	3V_S5
SYSTEM DC/DC MAX8717 37	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3
	1D05V_S0
TPS51100 39	
1D8V_S3	DDR_VREF
APL5312 39	
3D3V_S0	2D5V_S0
APL5912 38	
1D8V_S3	1D5V_S0

Intersil CHARGER MAX8731 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
	18V 4.0A
	UP+5V
	5V 100mA

CPU DC/DC MAX8770 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
	0-1.3V 48A

ICH7M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting PWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH7M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PCI Routing

	IDSEL	INT	REQ	GNT
OZ129	AD22	INT_PIRQ#	PCI_REQ#0	PCI_GNT#0

ICH7M Integrated Pull-up
and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

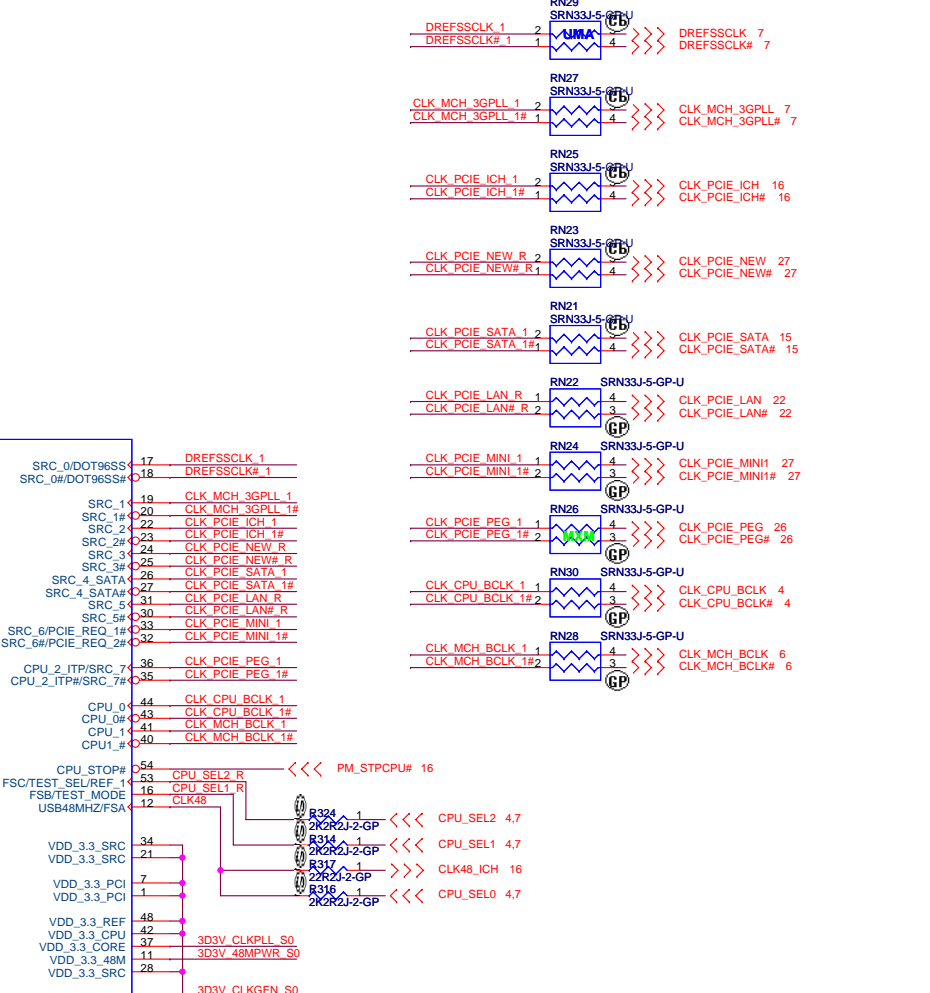
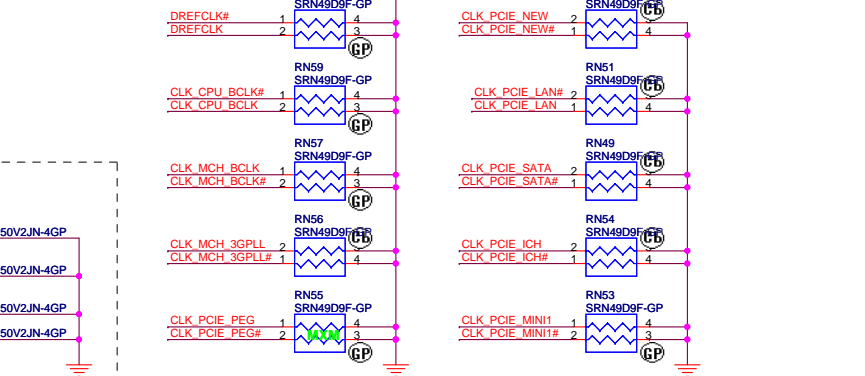
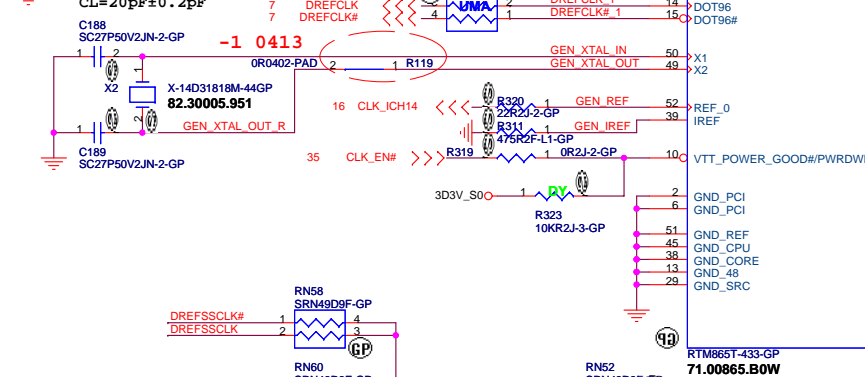
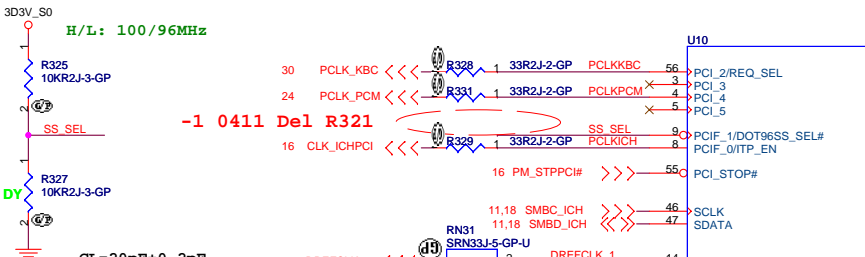
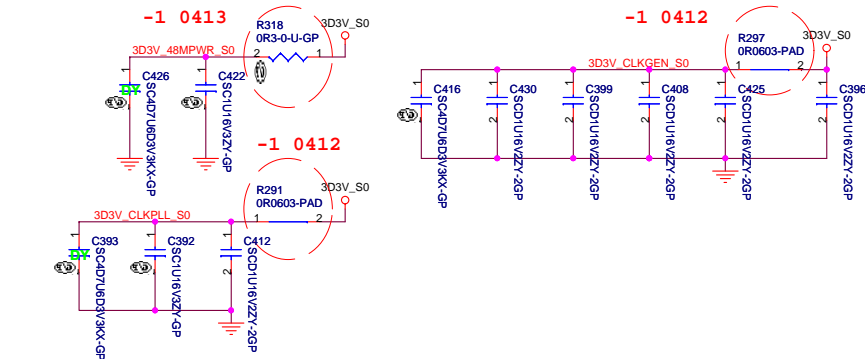
Crestline Strapping Signals and
Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWORK in signal.

UMA

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Title		
Reference		
Size A3	Document Number Volvi	Rev -1
Date: Wednesday, April 18, 2007	Sheet 2 of 42	



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

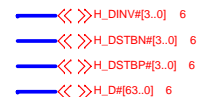
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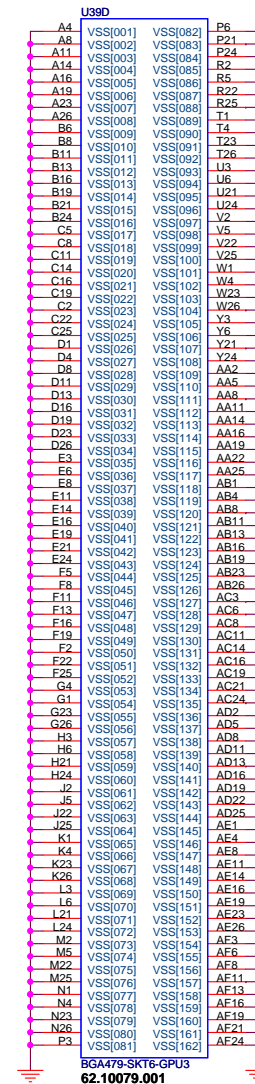
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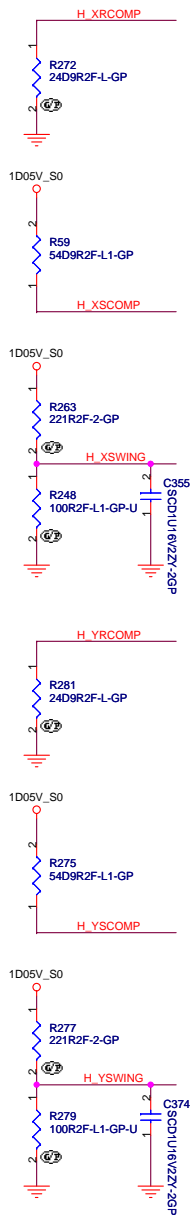
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Date: Wednesday, April 18, 2007 Sheet 3 of 42

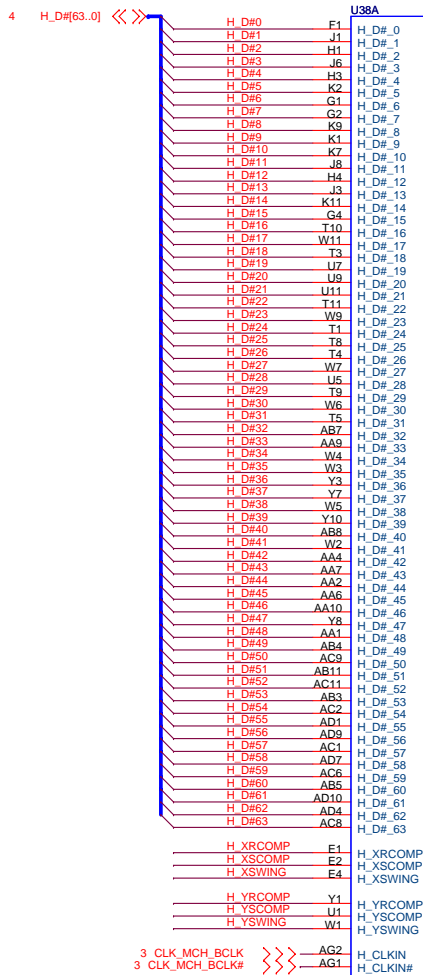


UMA			
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Title			
CPU (1 of 2)			
Size	Document Number	Rev	
Volvi		-1	
Date:	Wednesday, April 18, 2007	Sheet	4 of 42

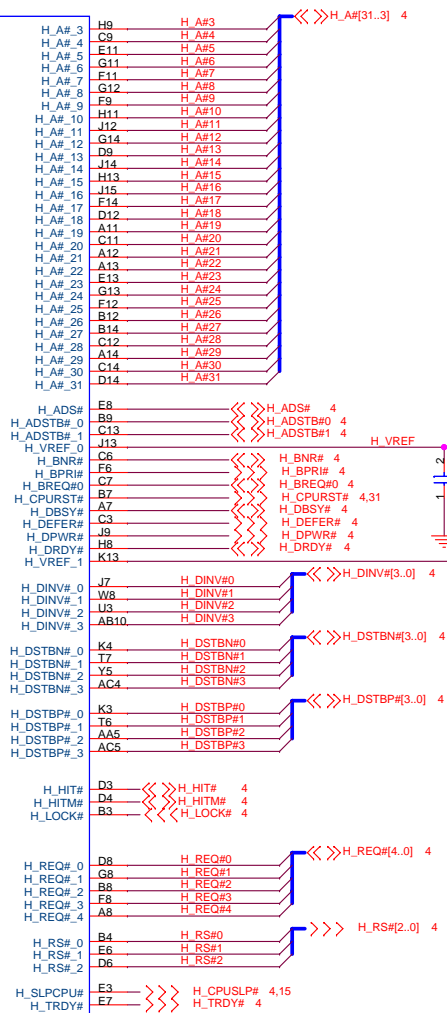




Place them near to the chip (< 0.5")

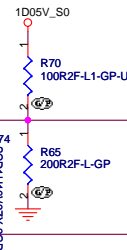


HSO7



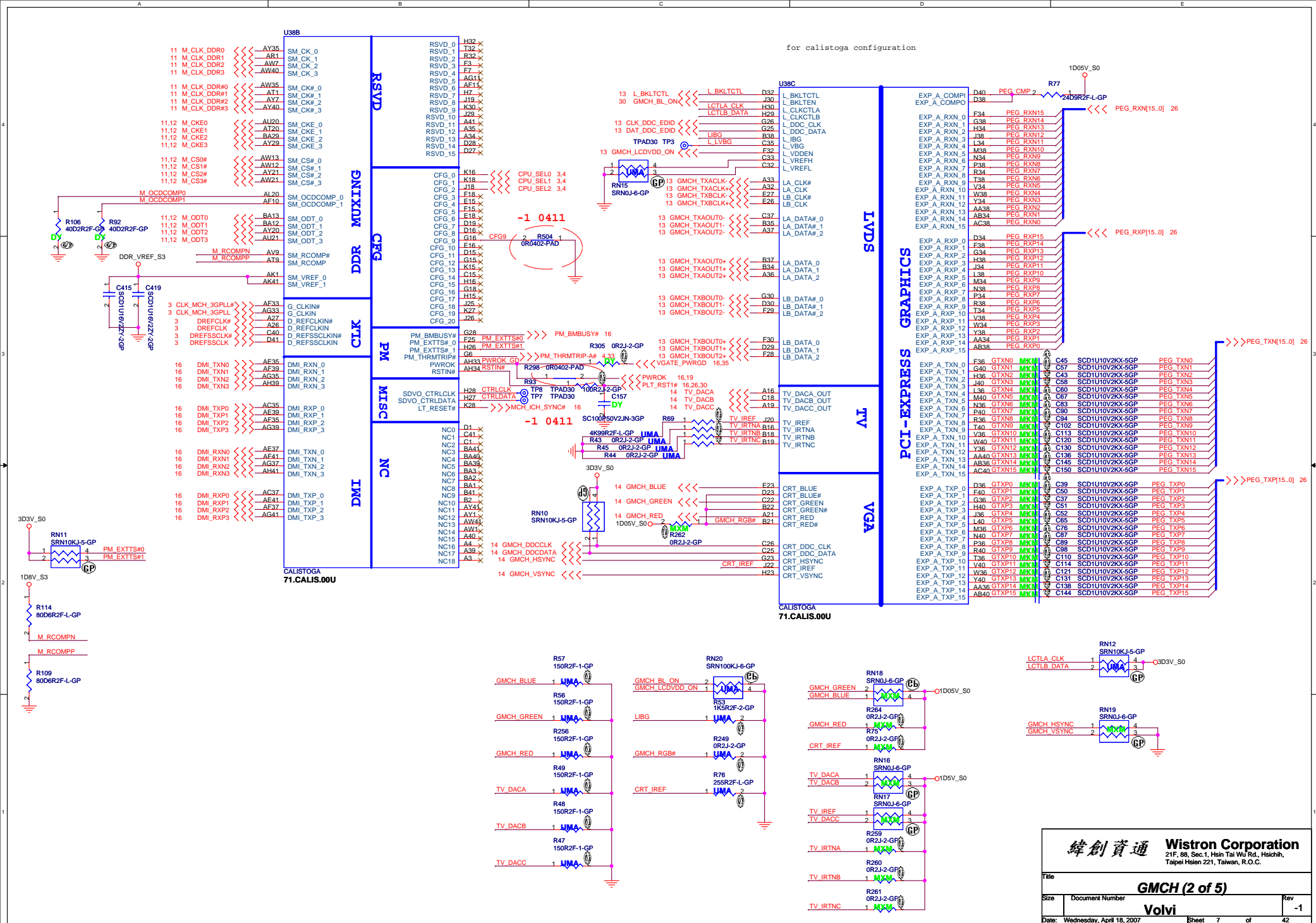
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71.CALIS.00U

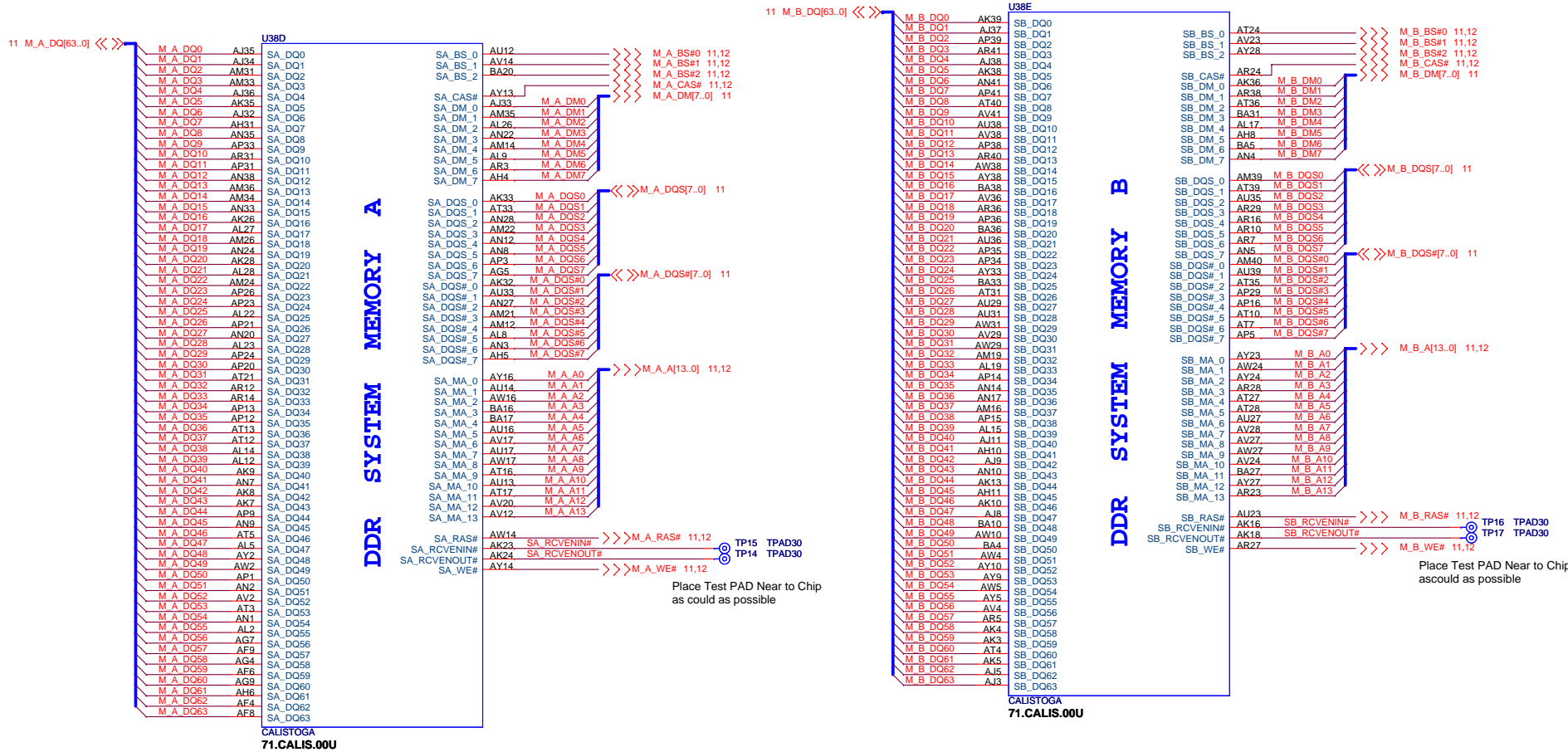
DIS :PM945 KI.94501.006
UMA :GM945 KI.94501.005



UMA

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Title	
GMCH (1 of 5)	
Size	Document Number
Volvi	
Date: Wednesday, April 18, 2007	Rev -1
Sheet 6	of 42

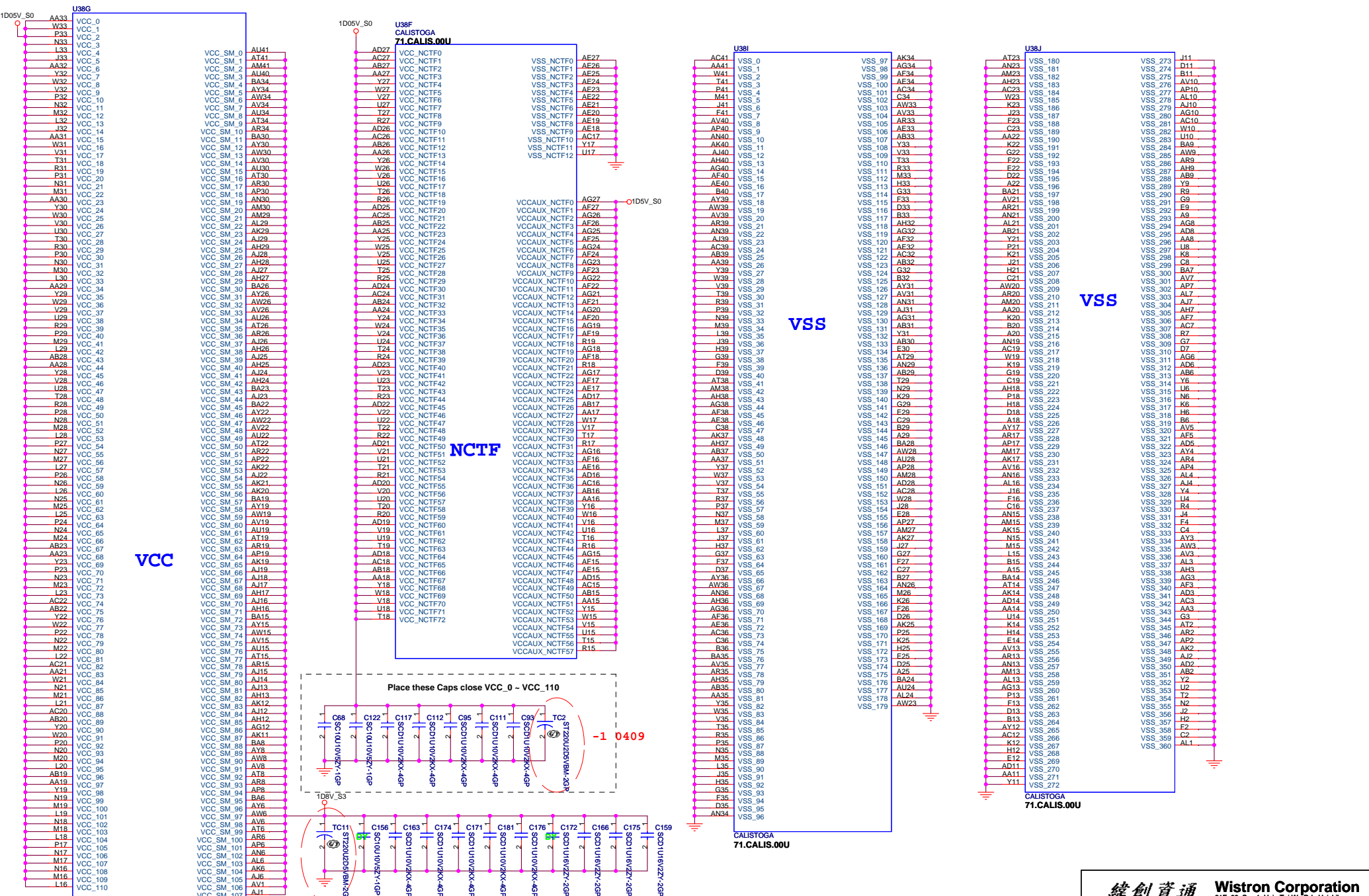




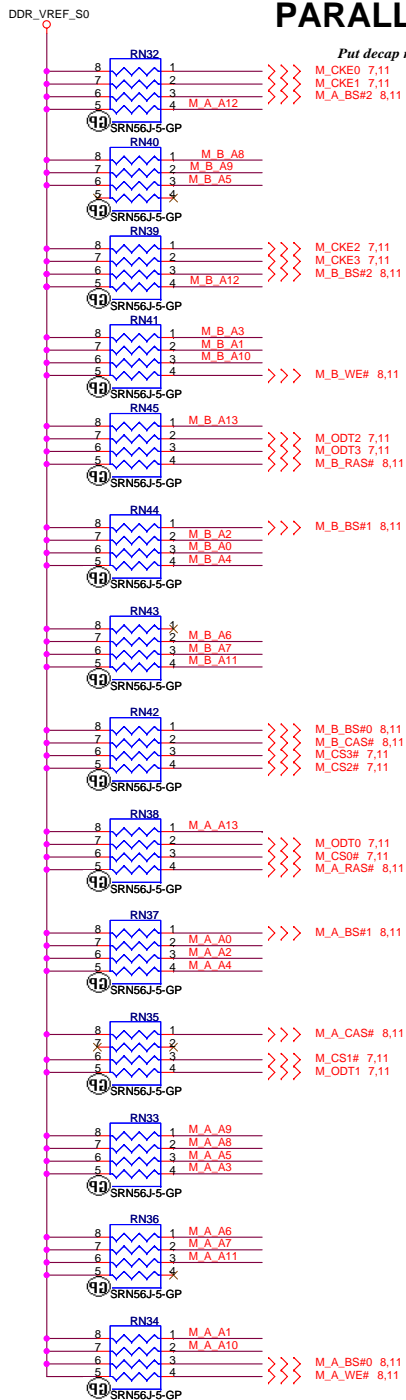
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Title		
GMCH (3 of 5)		
Size	Document Number	Rev
		-1
Date: Wednesday, April 18, 2007		
Sheet 8 of 42		

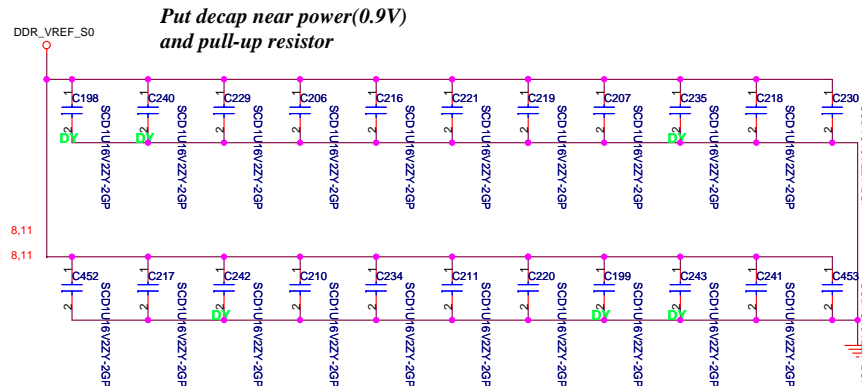
Volvi



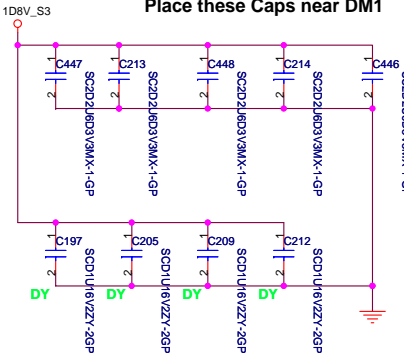
PARALLEL TERMINATION



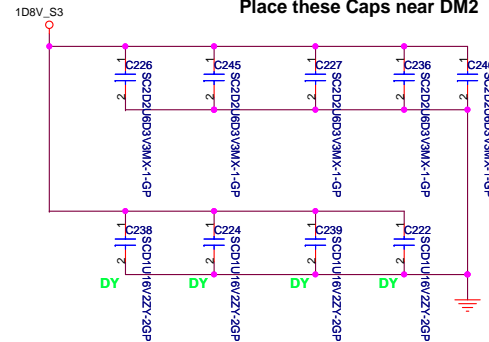
Decoupling Capacitor



Place these Caps near DM1

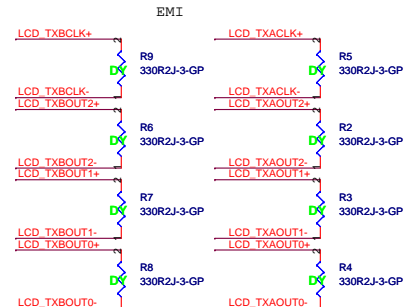
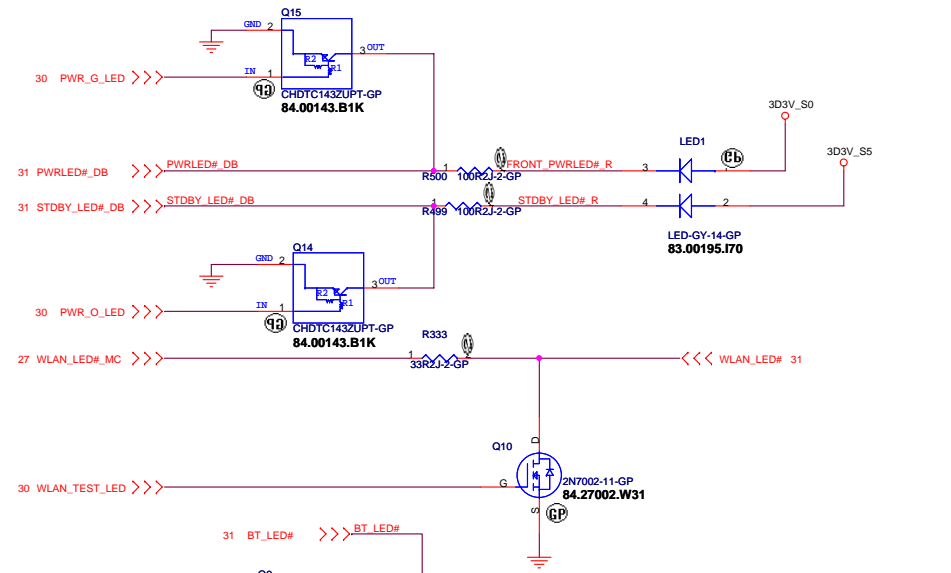


Place these Caps near DM2



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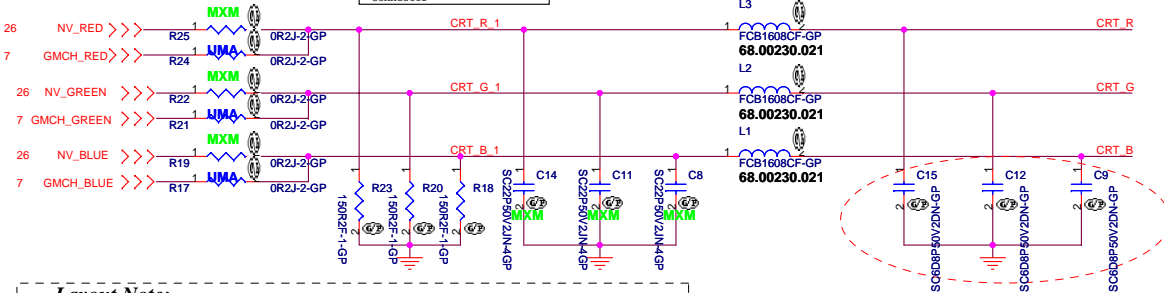
Title			
DDR2 Termination Resistor			
Size	Document Number		Rev
	Volvi		-1
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

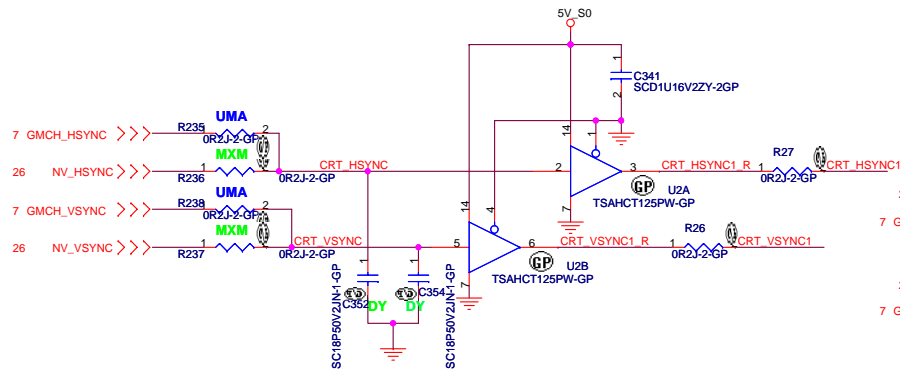
Ferrite bead impedance: 10 ohm@100MHz



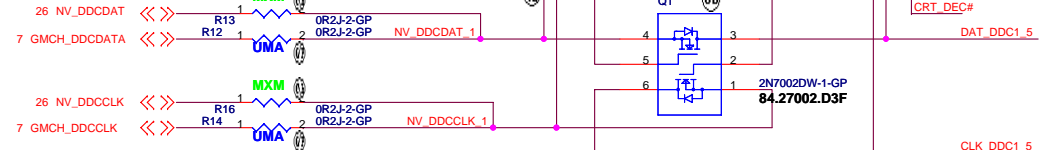
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

C15 to 18P
C12 to 27P
C9 to 27P
For ATI MXM M66M R,G,B

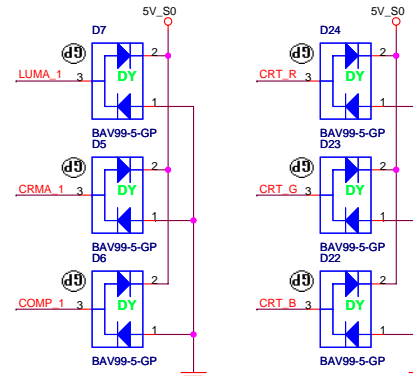
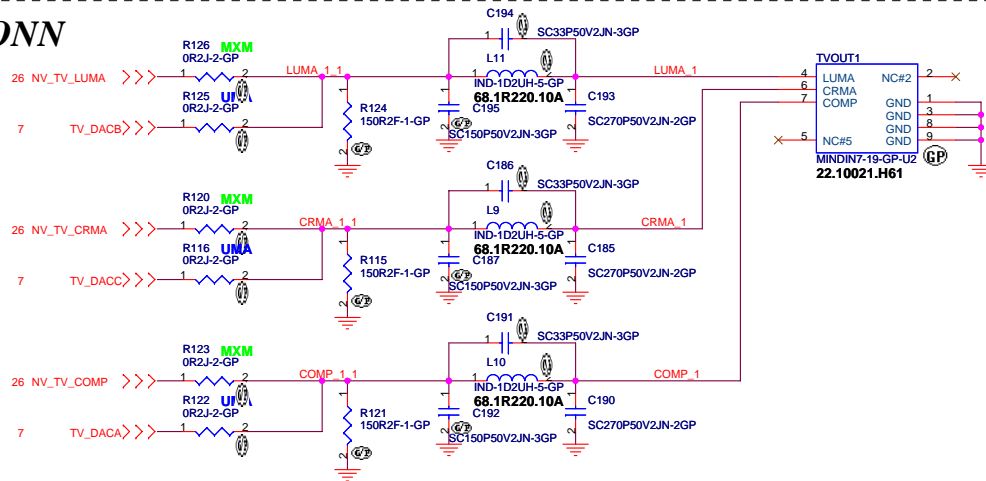
Hsync & Vsync level shift



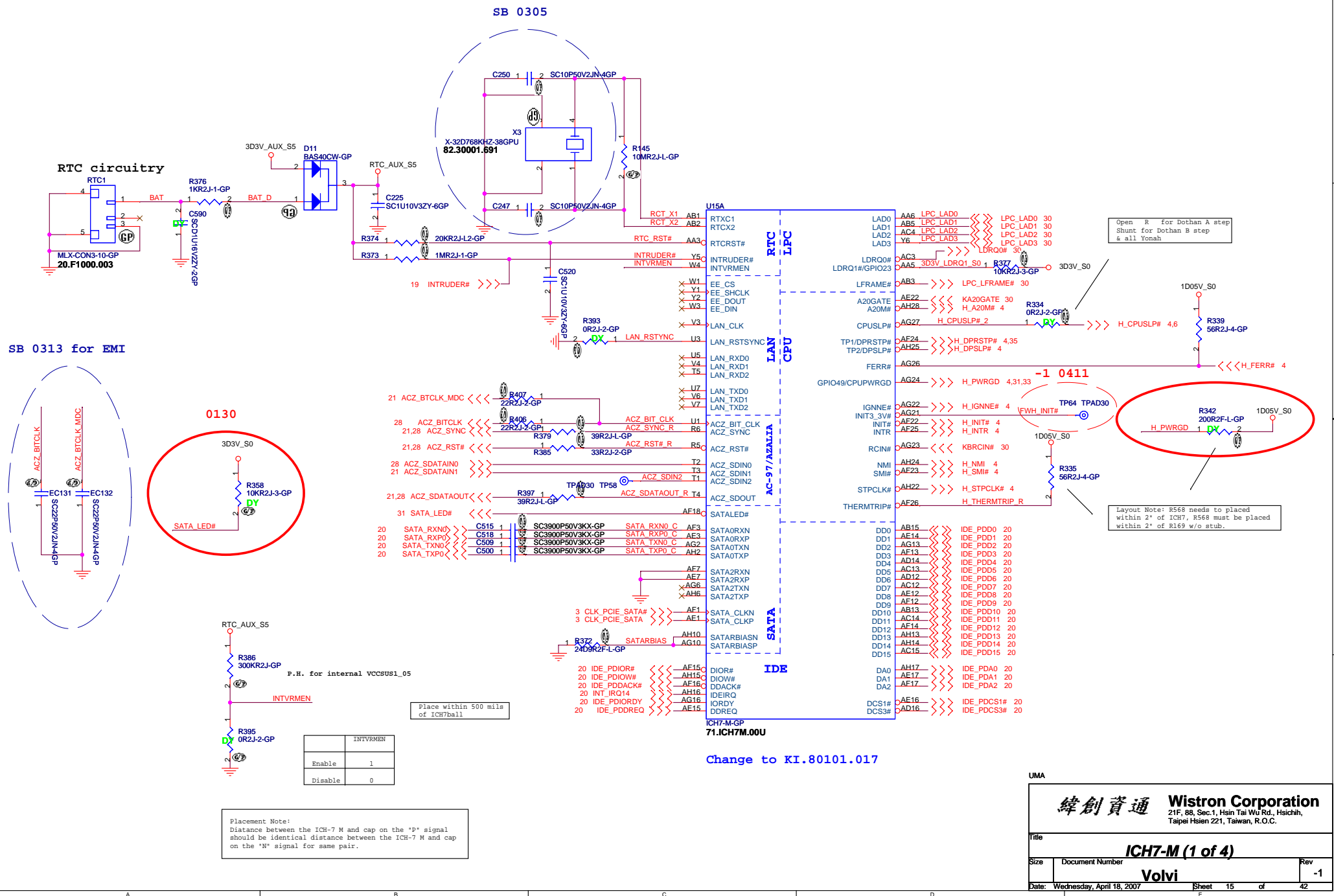
DDC_CLK & DATA level shift



TV CONN

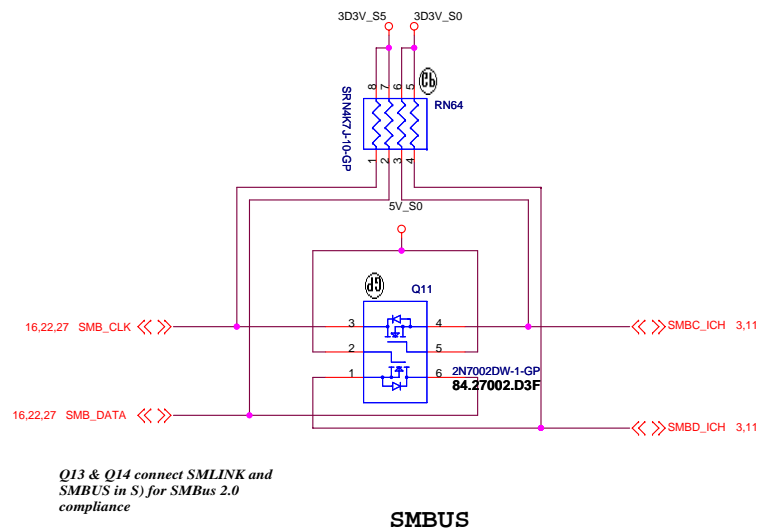


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Title CRT/TV Connector	
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Date: Wednesday, April 18, 2007	Sheet 14 of 42



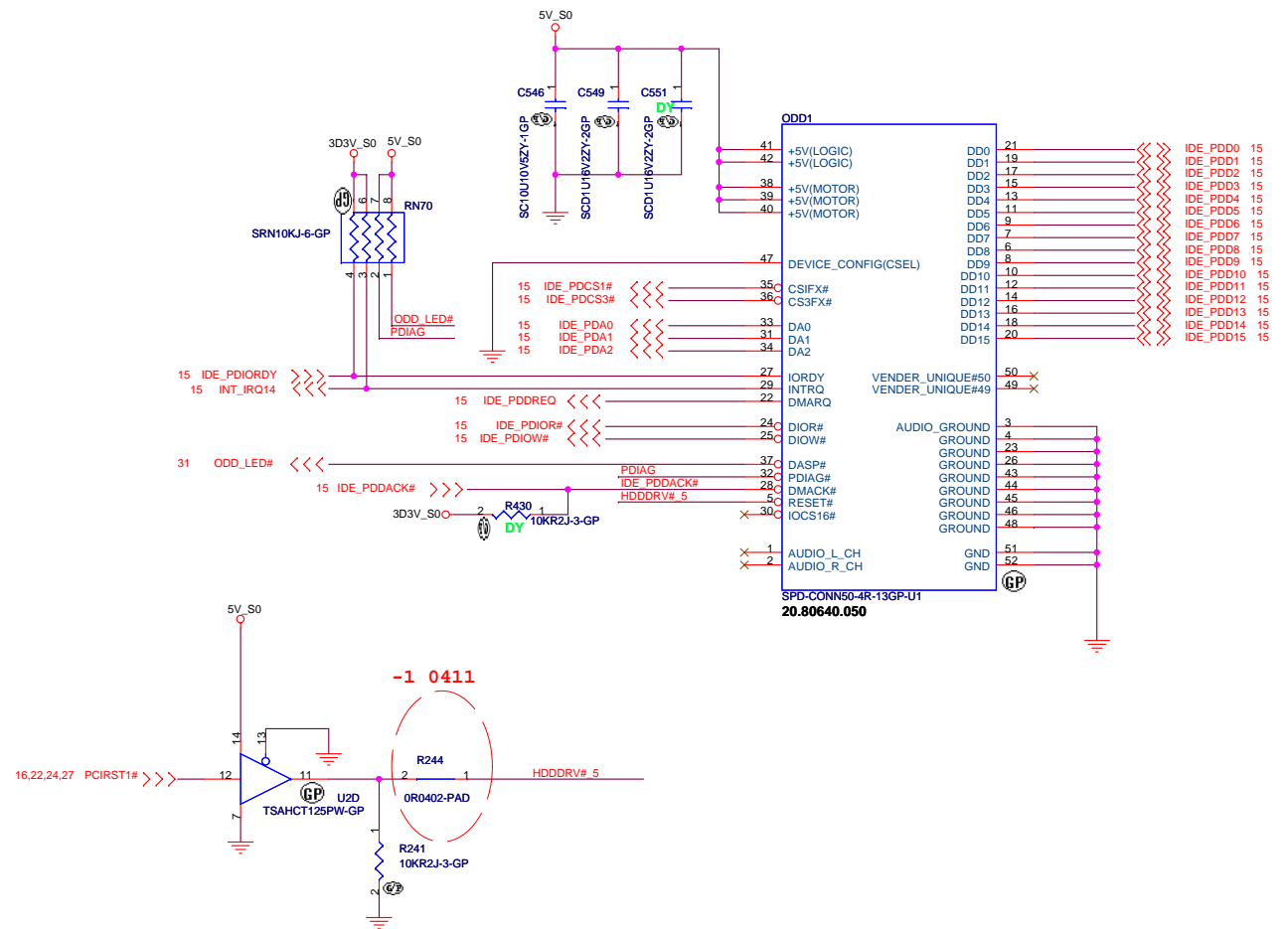
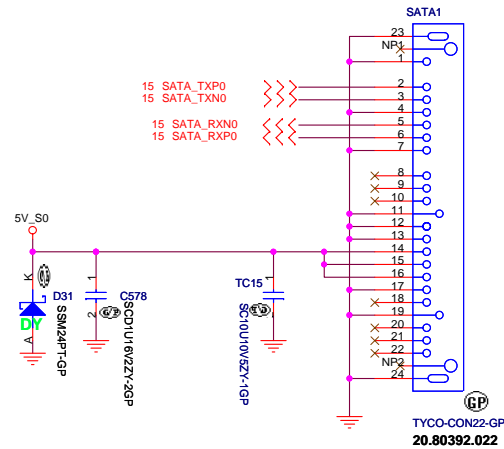
U15E			
A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B28	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J6	VSS[48]	VSS[145]	AB11
J24	VSS[49]	VSS[146]	AB14
J25	VSS[50]	VSS[147]	AB16
J26	VSS[51]	VSS[148]	AB19
K24	VSS[52]	VSS[149]	AB21
K27	VSS[53]	VSS[150]	AB24
K28	VSS[54]	VSS[151]	AB27
L13	VSS[55]	VSS[152]	AB28
L15	VSS[56]	VSS[153]	AC2
L24	VSS[57]	VSS[154]	AC5
L25	VSS[58]	VSS[155]	AC9
L26	VSS[59]	VSS[156]	AC11
M3	VSS[60]	VSS[157]	AD1
M4	VSS[61]	VSS[158]	AD3
M5	VSS[62]	VSS[159]	AD4
M12	VSS[63]	VSS[160]	AD7
M13	VSS[64]	VSS[161]	AD8
M14	VSS[65]	VSS[162]	AD11
M15	VSS[66]	VSS[163]	AD15
M16	VSS[67]	VSS[164]	AD19
M17	VSS[68]	VSS[165]	AD23
M24	VSS[69]	VSS[166]	AE2
M27	VSS[70]	VSS[167]	AE4
M28	VSS[71]	VSS[168]	AE8
N1	VSS[72]	VSS[169]	AE11
N2	VSS[73]	VSS[170]	AE13
N5	VSS[74]	VSS[171]	AE18
N6	VSS[75]	VSS[172]	AE21
N11	VSS[76]	VSS[173]	AE24
N12	VSS[77]	VSS[174]	AE25
N13	VSS[78]	VSS[175]	AF2
N14	VSS[79]	VSS[176]	AF4
N15	VSS[80]	VSS[177]	AF8
N16	VSS[81]	VSS[178]	AF11
N17	VSS[82]	VSS[179]	AF27
N18	VSS[83]	VSS[180]	AF28
N24	VSS[84]	VSS[181]	AG1
N25	VSS[85]	VSS[182]	AG3
N26	VSS[86]	VSS[183]	AG7
P3	VSS[87]	VSS[184]	AG11
P4	VSS[88]	VSS[185]	AG14
P12	VSS[89]	VSS[186]	AG17
P13	VSS[90]	VSS[187]	AG20
P14	VSS[91]	VSS[188]	AG25
P15	VSS[92]	VSS[189]	AH1
P16	VSS[93]	VSS[190]	AH3
P17	VSS[94]	VSS[191]	AH7
P24	VSS[95]	VSS[192]	AH12
P27	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27

ICH7-M-GP
71.ICH7M.00U



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Title			
ICH7-M (4 of 4)			
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ODD Connector



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Title

HDD and CDROM

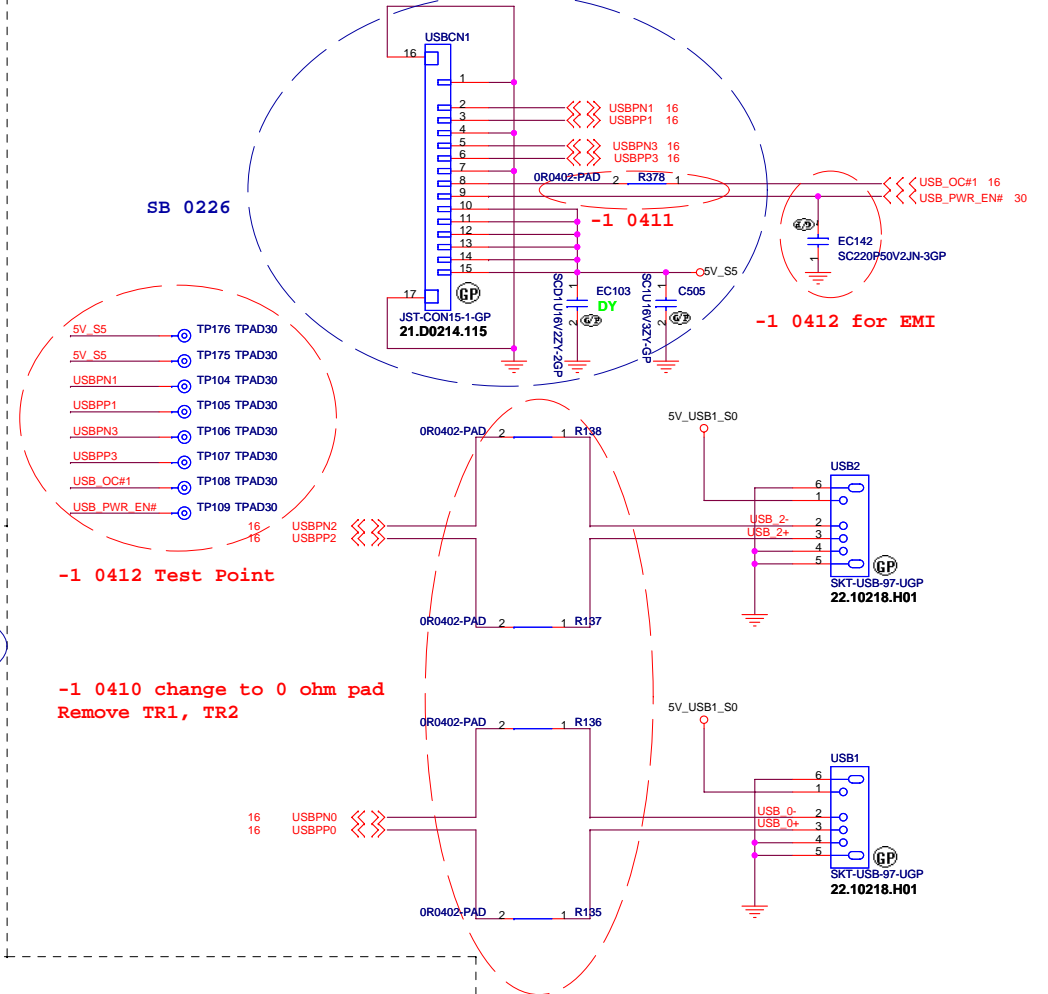
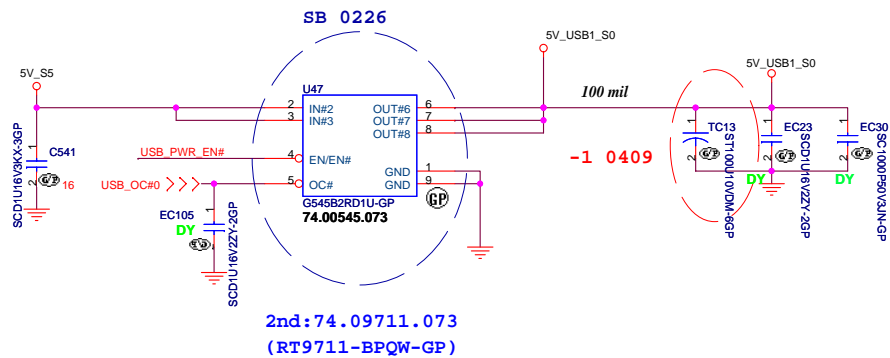
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Volvi

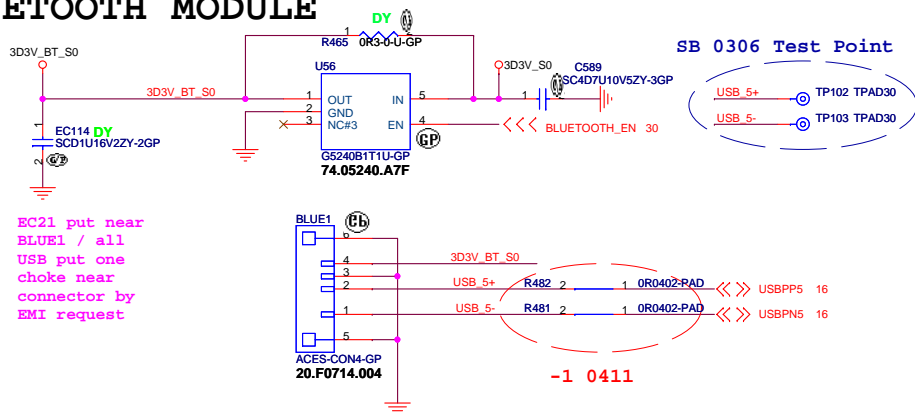
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Date: Wednesday, April 18, 2007

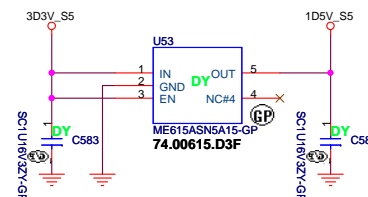
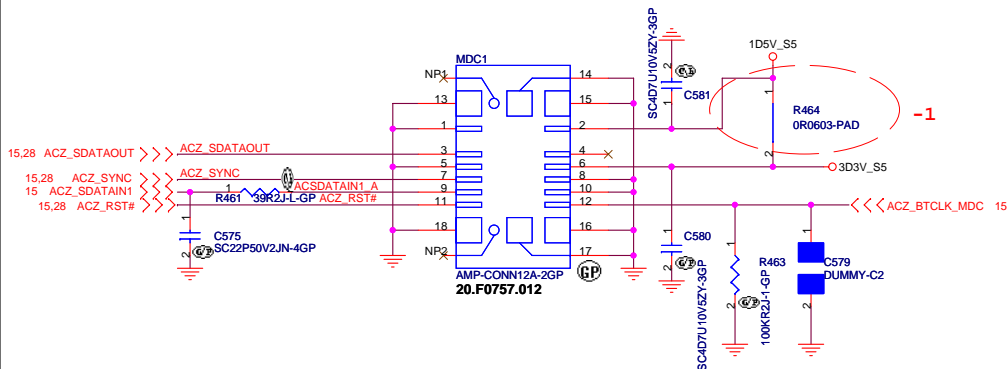
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BLUETOOTH MODULE

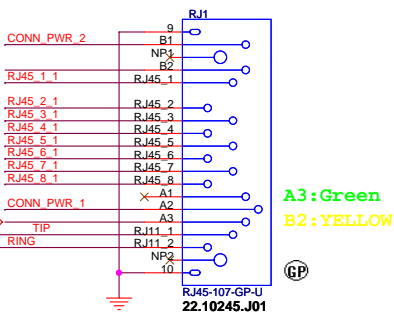
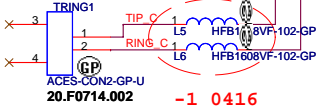
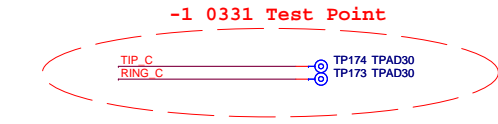


MDC 1.5 CONN

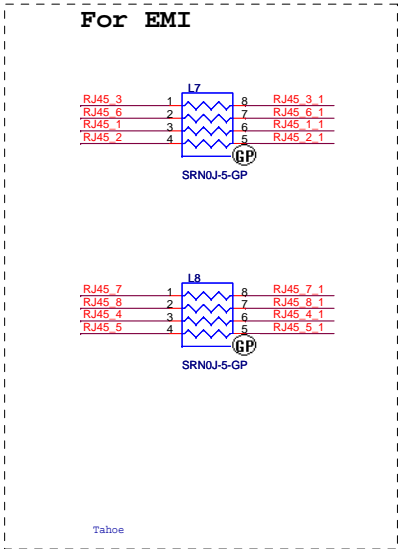
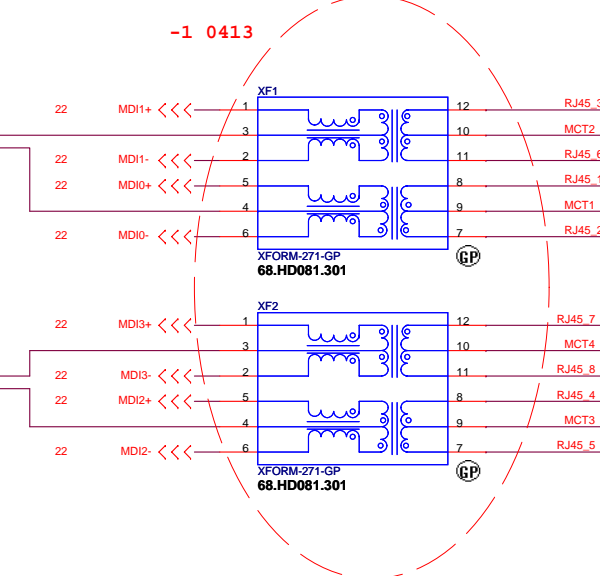


Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



GIGA Lan Transformer

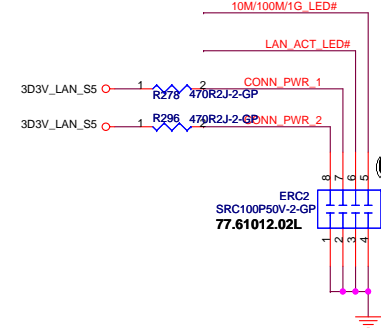
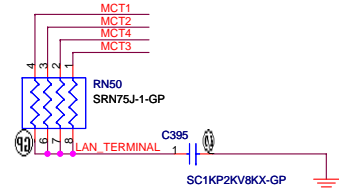


- 1.route on bottom as differential pairs.
- 2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



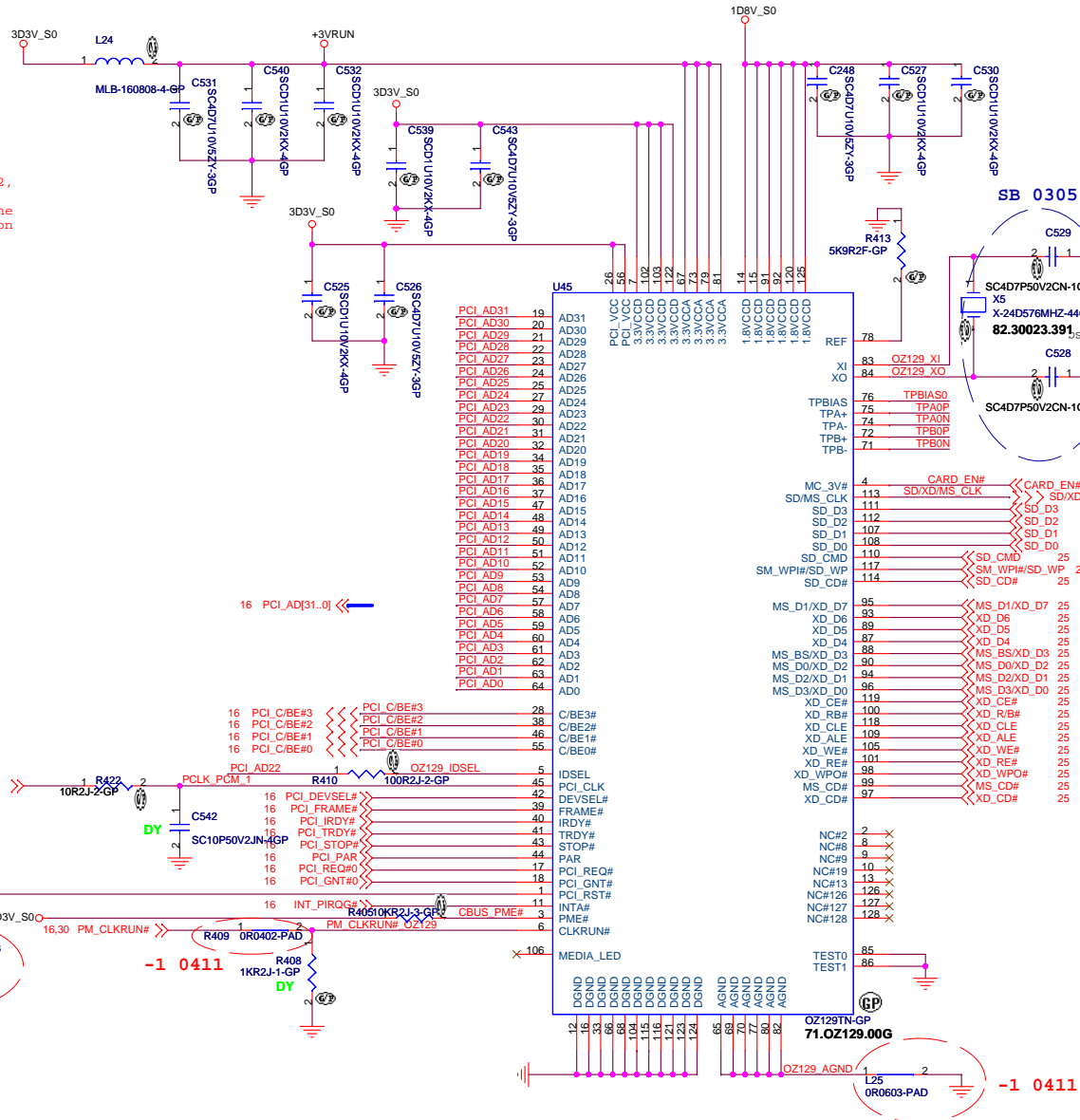
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Title: **LAN Connector**

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TPB1A0P		TPB1A0P	25
TPA0P	↔	TPA0P	25
TPA0N	↔	TPA0N	25
TPB0P	↔	TPB0P	25
TPB0N	↔	TPB0N	25

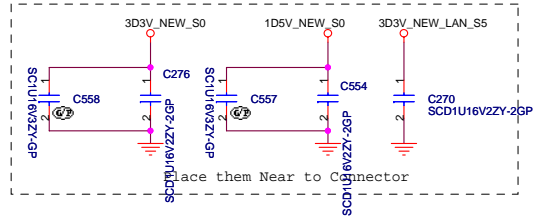
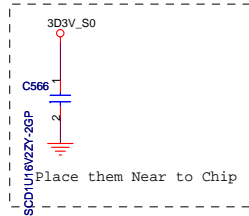
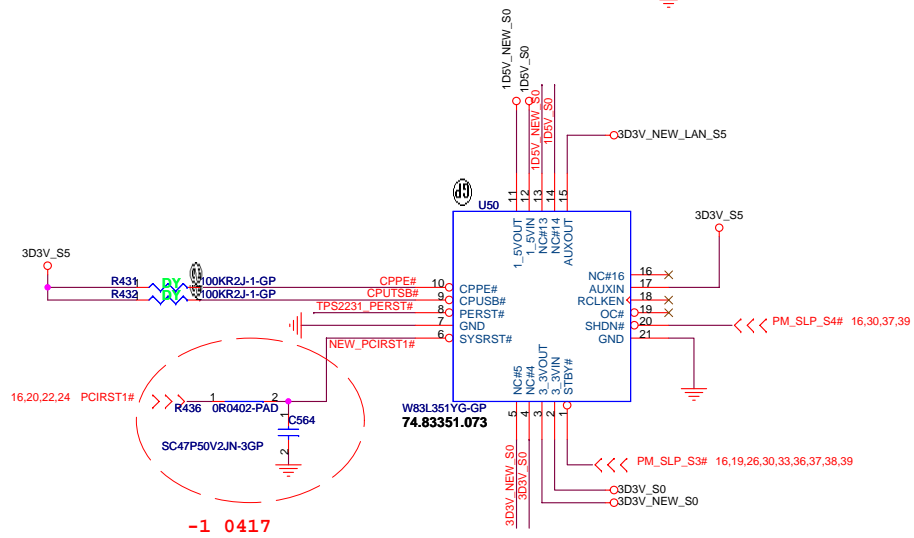
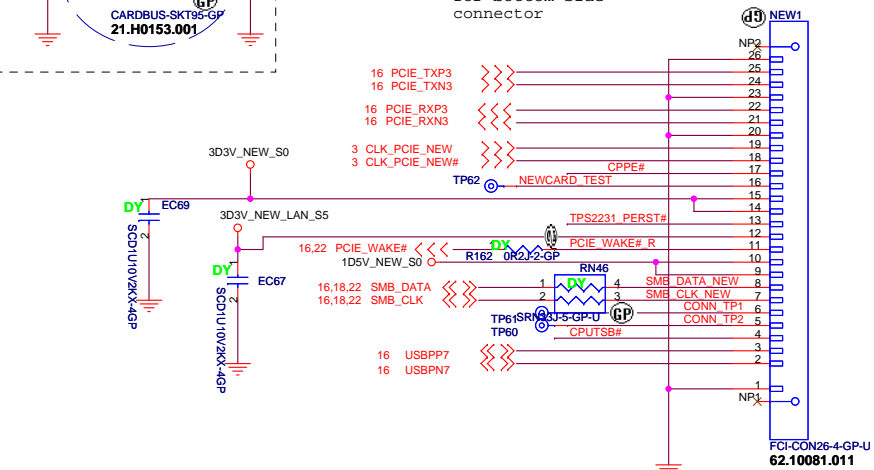
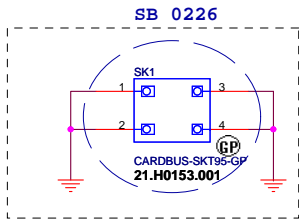
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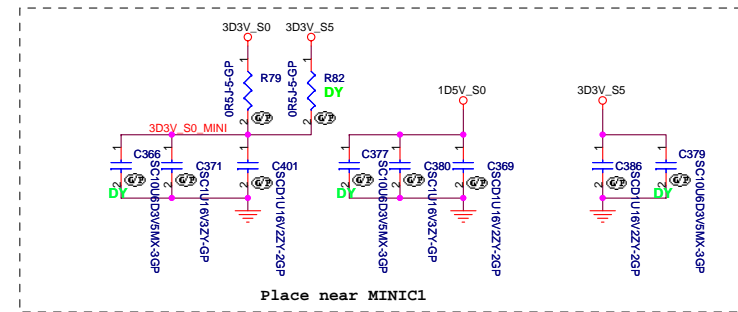
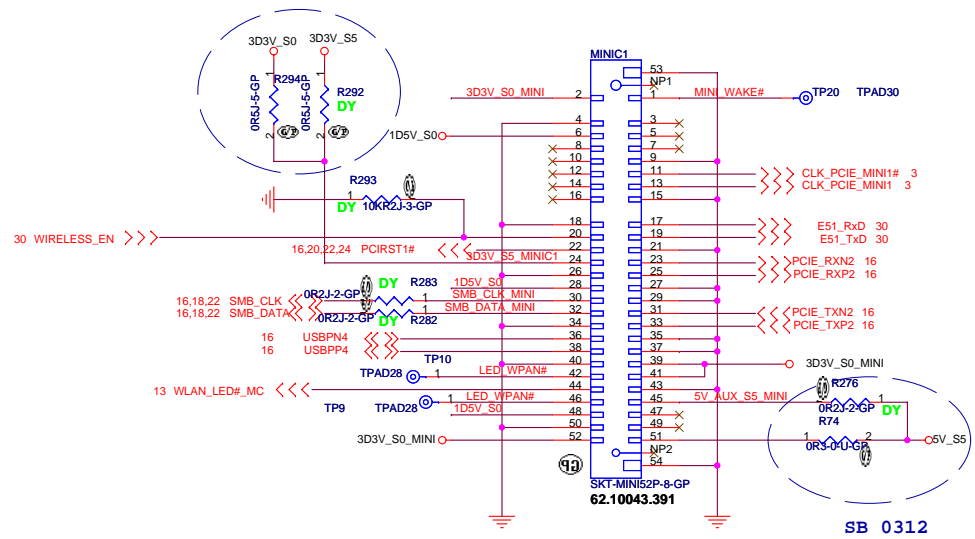
Mini Card Connector

NEWCARD Connector

Reserve the symbol
for bottom side
connector



SB 0312



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Title

MINI CARD / NEW CARD

Size

Document Number	
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Volvi

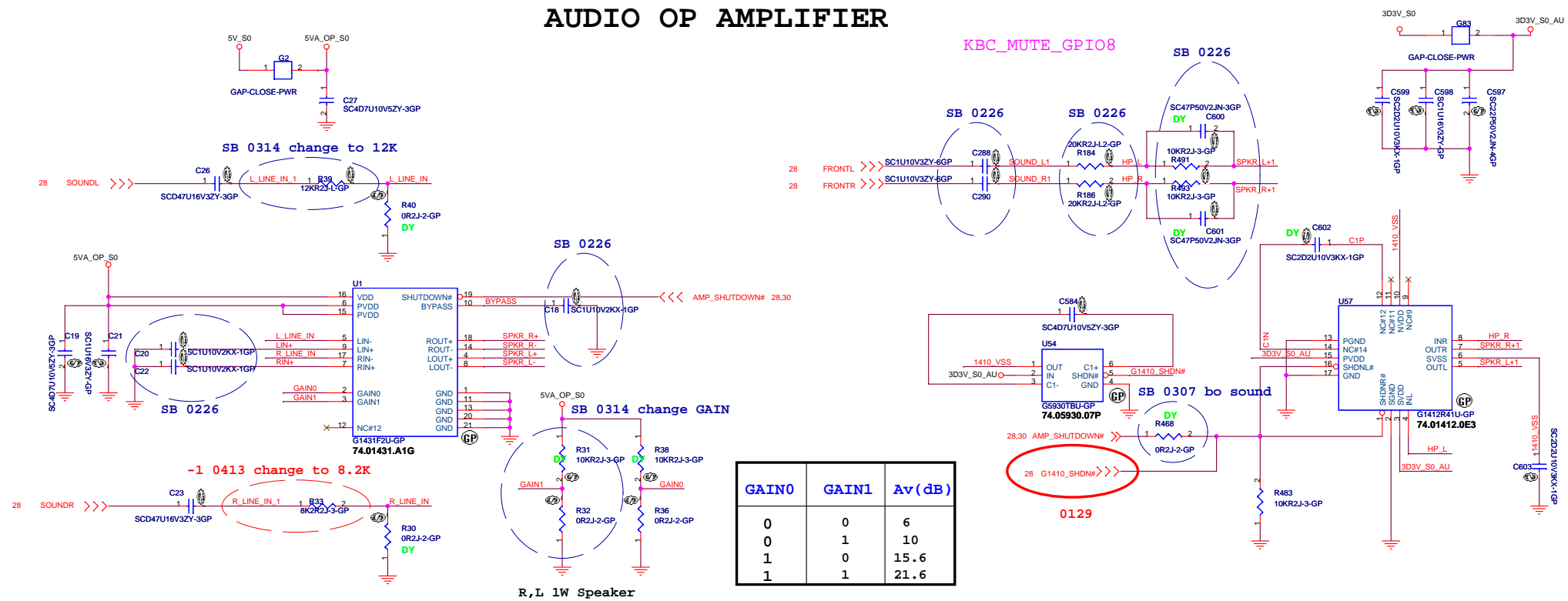
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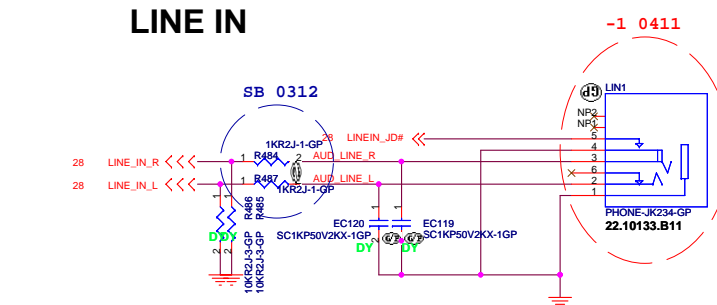
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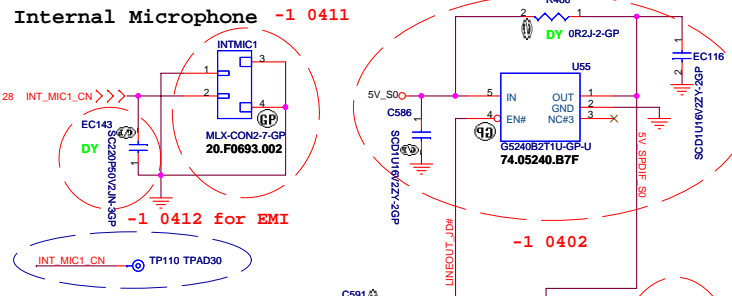
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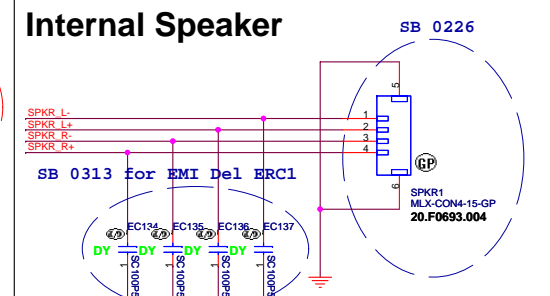
LINE IN



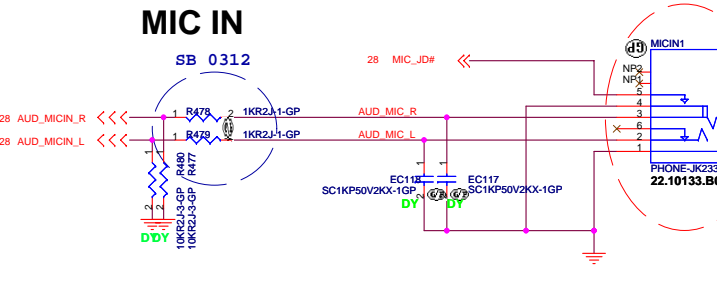
Internal Microphone -1 0411



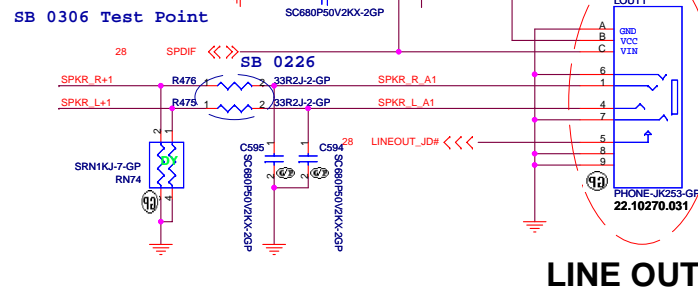
Internal Speaker



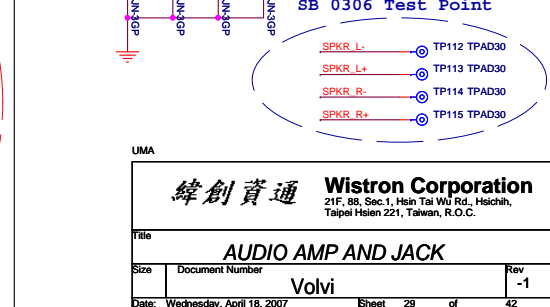
MIC IN

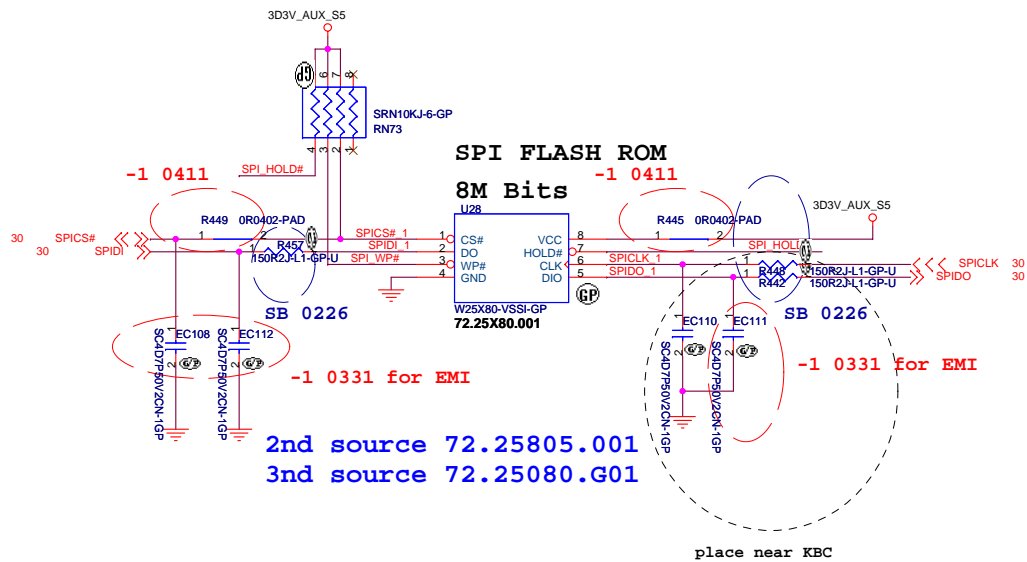


SB 0306 Test Point



LINE OUT



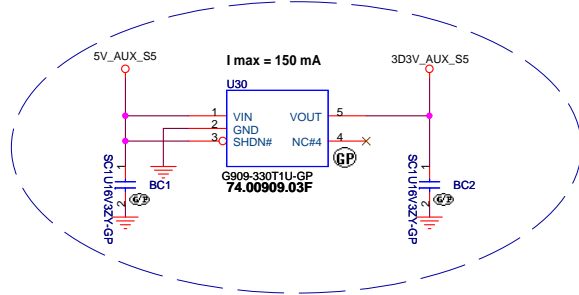


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BIOS			
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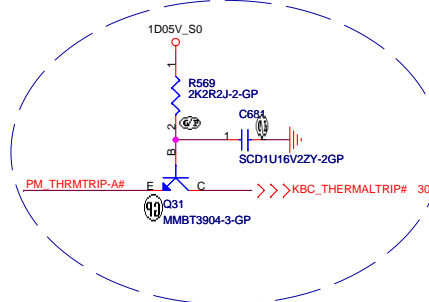
Aux Power

3D3V_AUX_S5

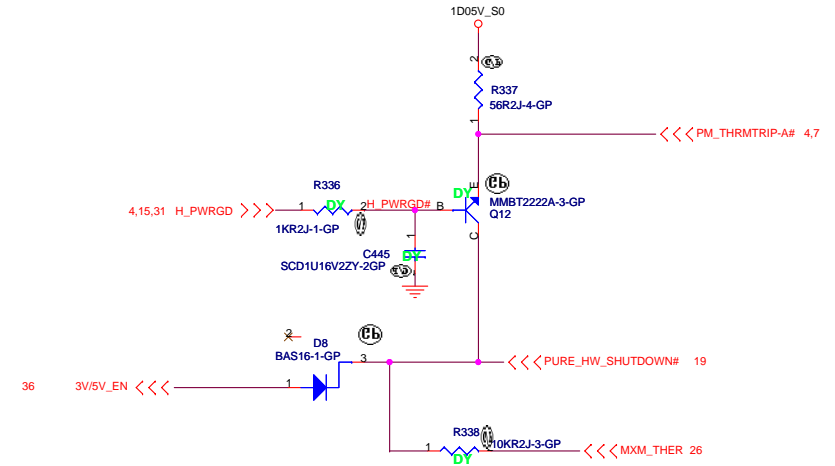
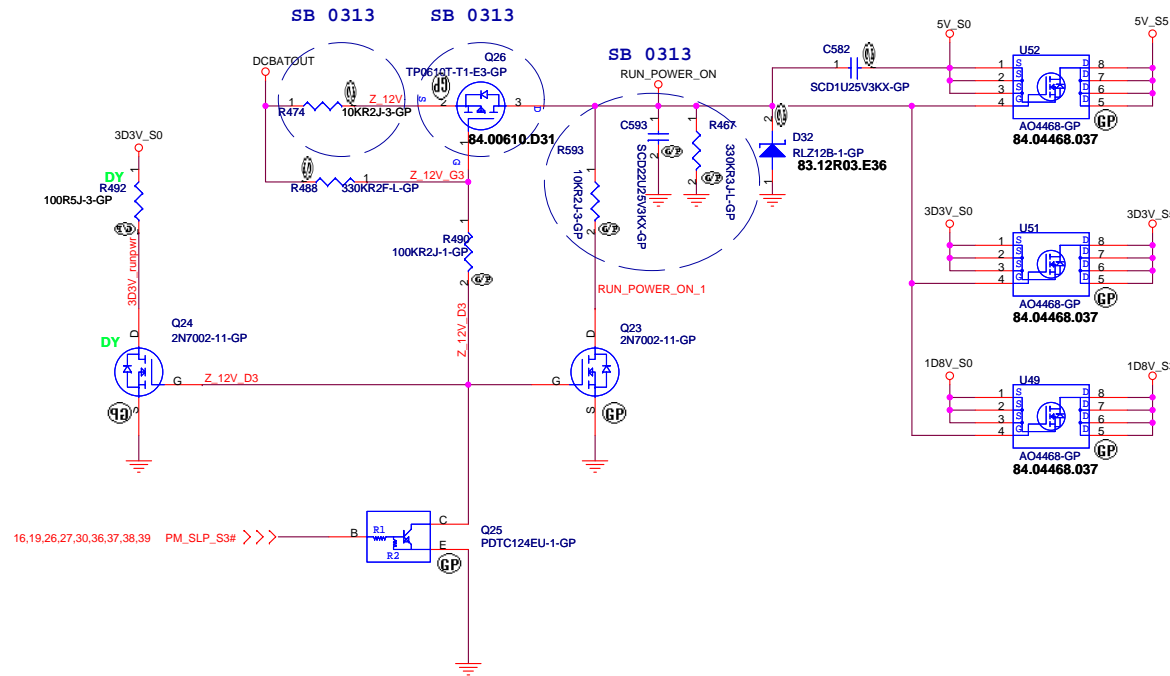


SB 0226 Del R458,R460,BC3 (SA)

SB 0216



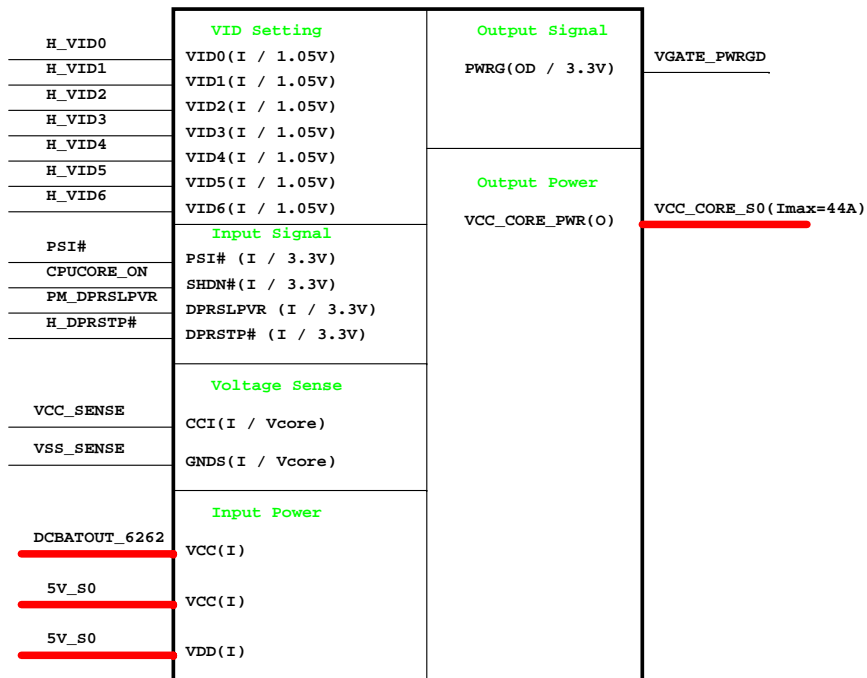
Run Power



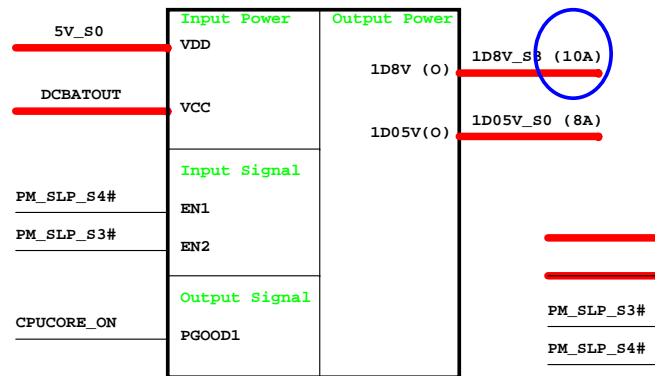
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RUN POWER and 3D3V_AUX_S5			
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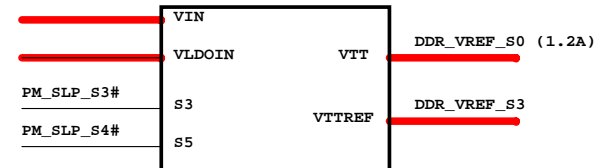
**CPU_CORE
MAX8770**



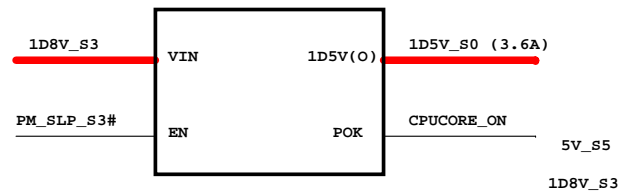
**MAX8717
1D8V_S3 / 1D05V_S0**



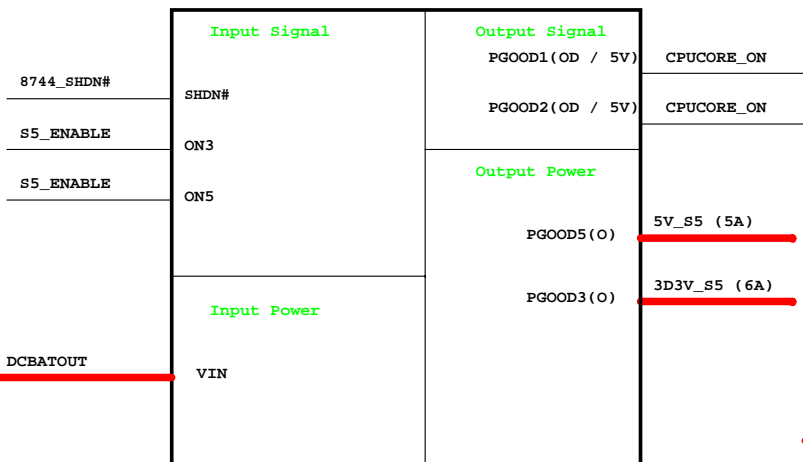
**TPS51100
DDR_VREF_S0**



**APL5912
1D5V_S0**



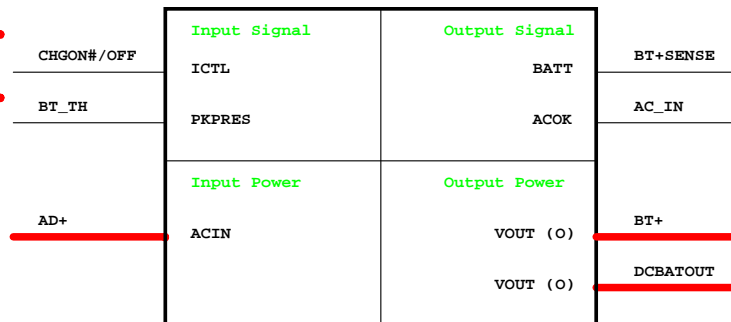
**MAX8744
5V_S5 / 3D3V_S5**



**APL5312
2D5V_S0**

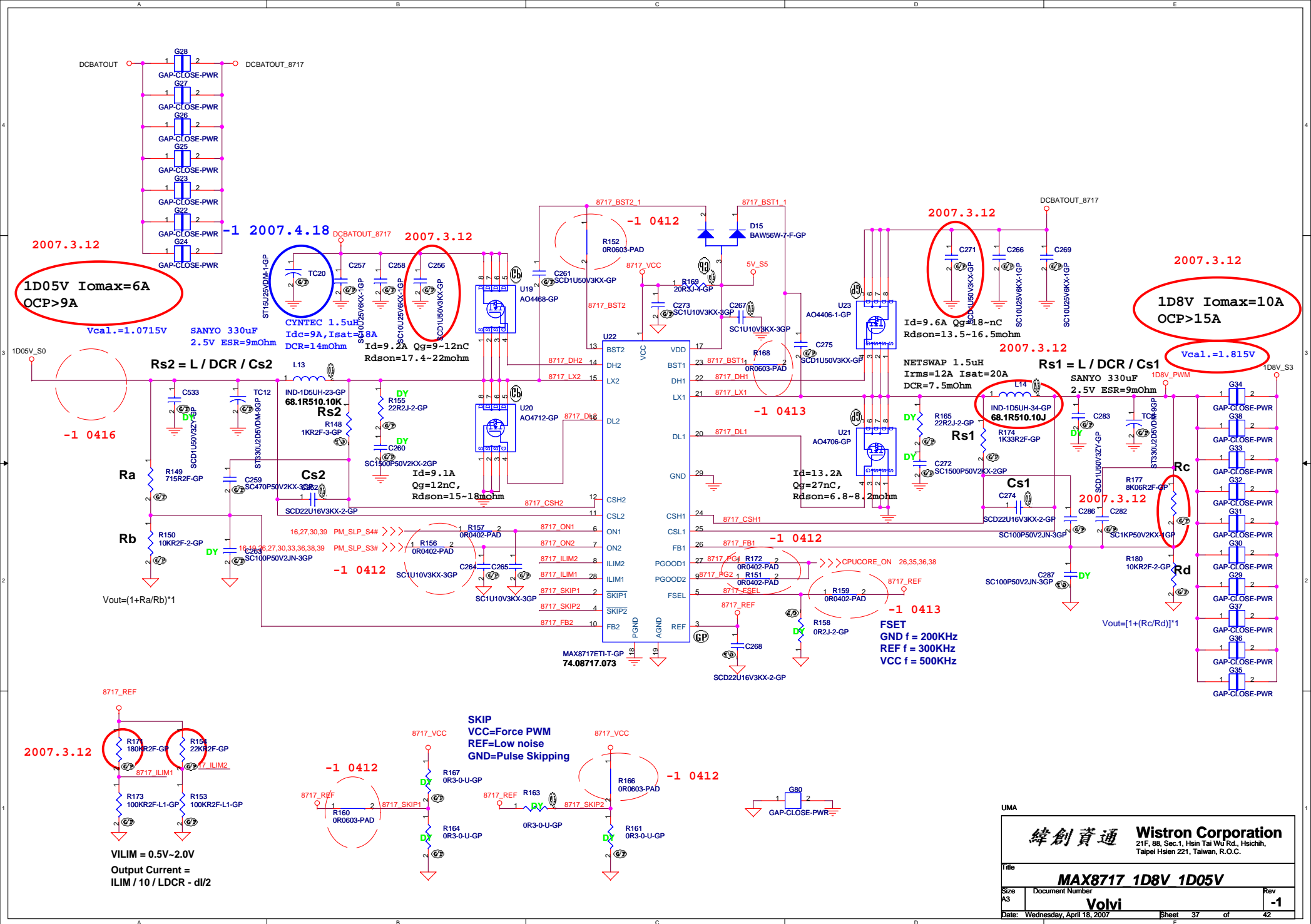


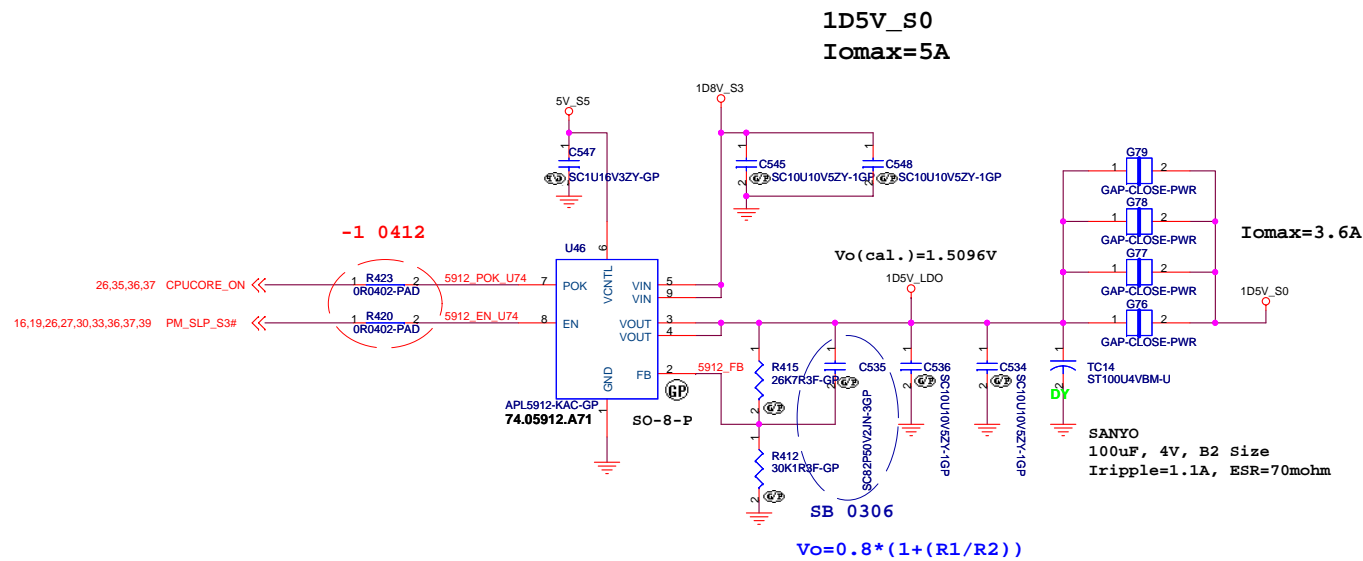
Charger MAX8731A



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Power Block Diagram	
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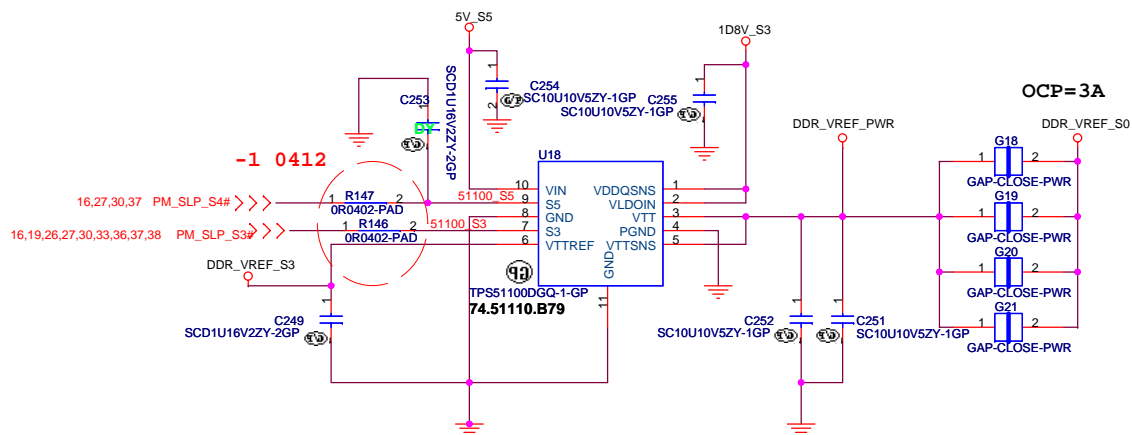




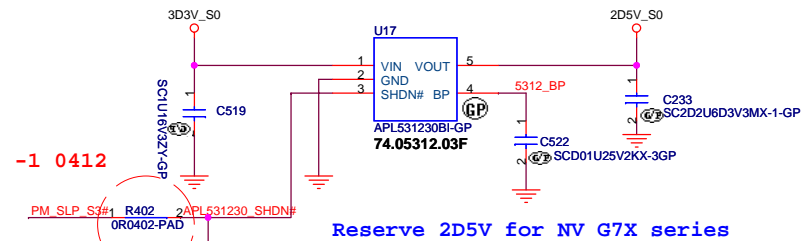
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APW5912_1D5V	
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0D9V_S3 Iomax=0.5A



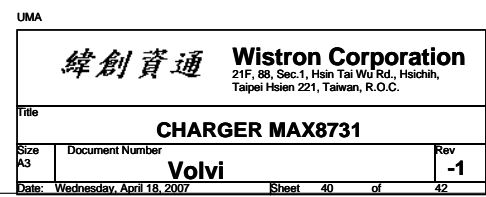
2D5V Iomax=130mA



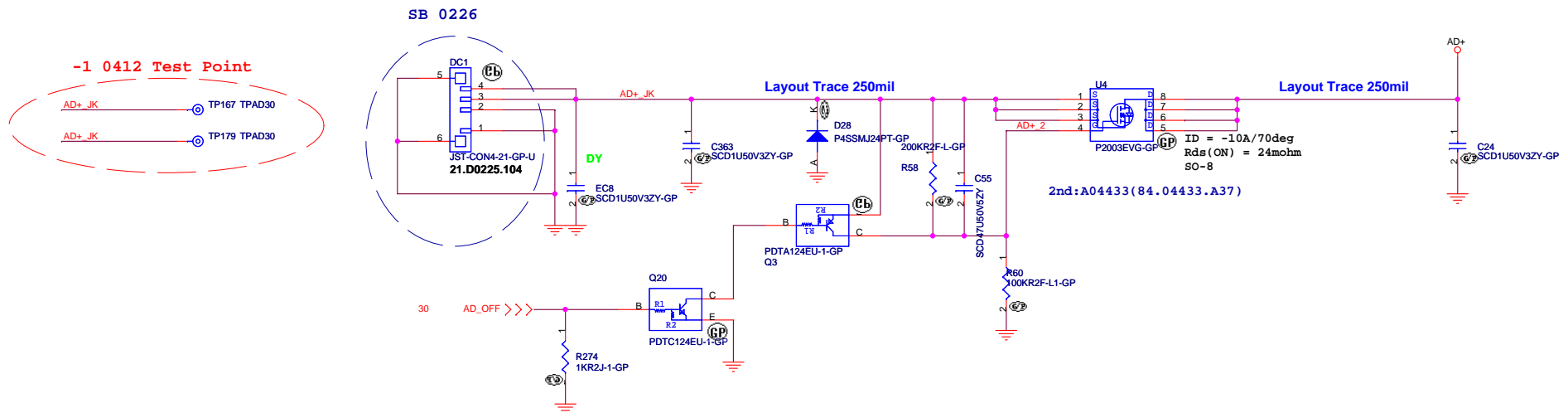
Reserve 2D5V for NV G7X series

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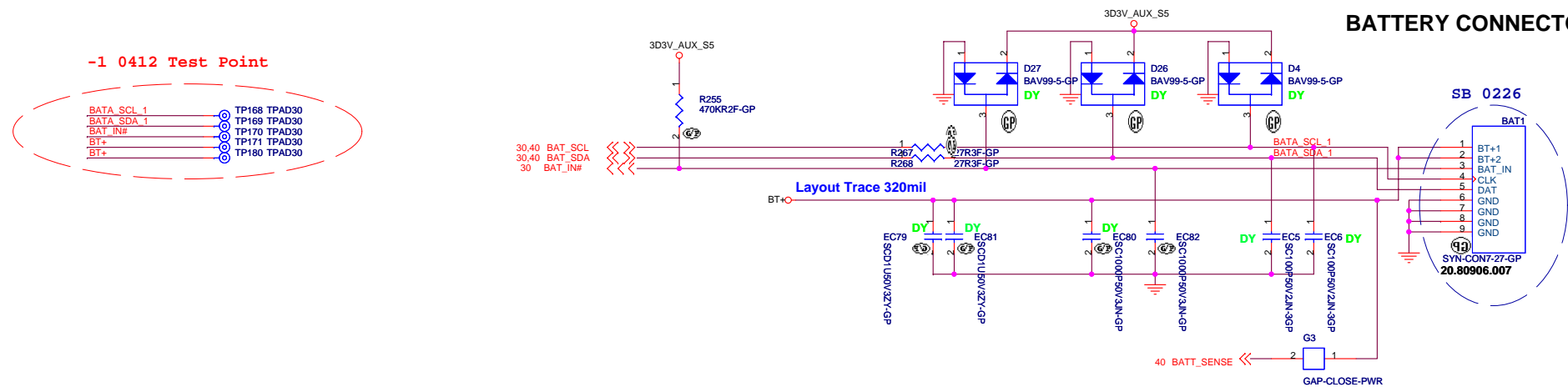
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Title			
2D5V / 0D9V			
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Adaptor in to generate DCBATOUT



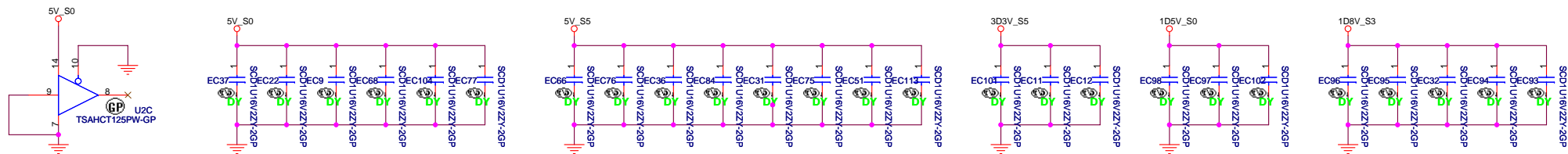
BATTERY CONNECTOR



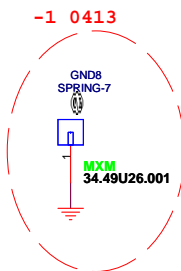
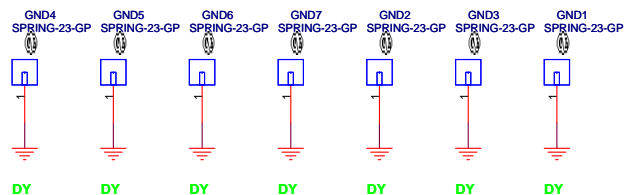
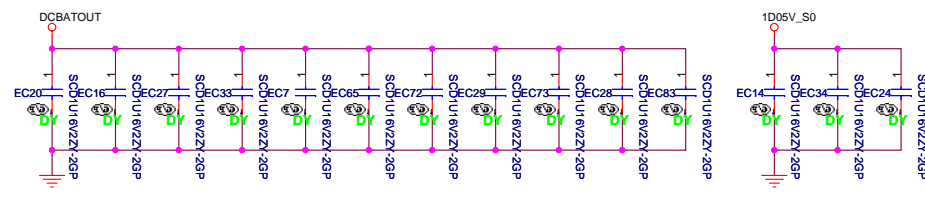
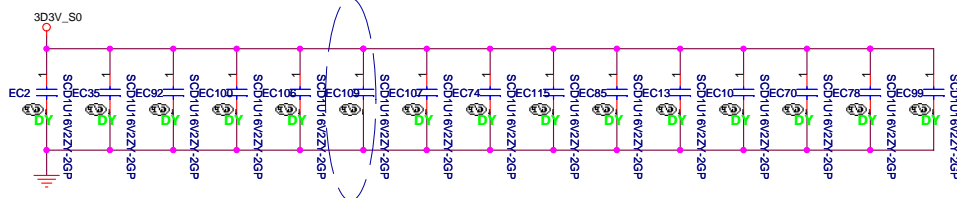
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Taipei Hsien 221, Taiwan, R.O.C.

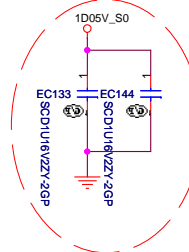
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Size	Document Number	Rev
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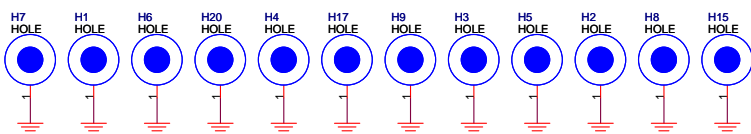
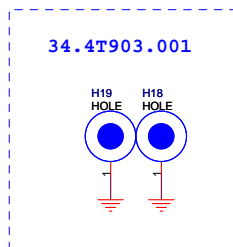
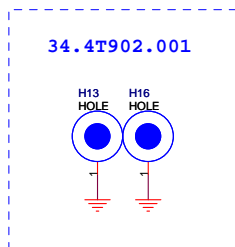
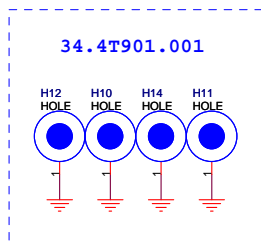
SB 0312 for EMI



-1 0417 for EMI



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EMI/Spring/Boss	
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